Partial English Translation of

LAID OPEN unexamined

JAPANESE PATENT APPLICATION

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[0008] to [0016]

[0008]

[Embodiments]

(First Embodiment) Figure 1 shows a semiconductor device fabrication method according to the present invention. Firstly, a polysilicon gate pattern is formed on a Si substrate 1 of which active region is defined by a LOCOS oxide film 2 and which has a p-well region 3 formed by B doping. More specifically, after a gate oxide film 4 is formed to 10 nm on the active region, a polysilicon film 5 is formed to 250 nm thereon and then, is processed into the gate electrode pattern by photoetching (Figure a).

[0009] A thermal CVD-SiO_2 film 6 is formed to 100 nm on the Si substrate (Figure b). The thermal CVD-SiO_2 film 6 is etched by an anisotropic dry etching technique to remove the part of the thermal CVD-SiO_2 film 6 other than a side spacer 7 (Figure c).

[0010] A thermal CVD-SiO_2 film 8 as an implantation through film is formed to 10 nm on the entire surface of the Si substrate, and As ions are implanted into the source/drain regions and the gate electrode, which are not covered with the LOCOS oxide film 2, at one time. Then, the thus implanted As ions are activated by rapid heating at a temperature of 950 ℃ for 10 seconds so that a n^+ diffusion layer 9 is formed (Figure d).

[0011] After the CVD-SiO_2 film 8 as the implantation through film is wet removed, a Co film 10 is formed to 5 nm on the entire surface of the substrate by a DC magnetron sputtering method and a TiN film 11 is formed to 10 nm thereon (Figure e).

[0012] A thermal treatment is performed under a nitrogen atmosphere at a temperature of 550 ℃ for 30 seconds and a cobalt silicide layer 12 is selectively formed only on the electrode where Co and Si are in contact with each other. Herein, cobalt silicide has a composition ratio Co : Si of 1 : x ($x \leqq 1$).

[0013] After the non-reacting Co film and the non-reacting TiN film are removed by wet etching, a thermal treatment is performed under a nitrogen atmosphere at a temperature of 750 ℃ for 30 second so that the cobalt silicide layer 12 is converted into a stoichiometric compound ($CoSi_2$) in which Co : Si is 1 : 2 (Figure g). Finally, the cobalt silicide layer 12 has a thickness of 17 nm.

[0014] A Co film 13 is formed again to 5 nm on the entire surface of the substrate by a DC magnetron sputtering method and a TiN film 14 is formed to 10 nm thereon (Figure h).

[0015] A thermal treatment is performed under a nitrogen atmosphere at a temperature of 550 ℃ for 30 seconds so that a cobalt silicide layer is selectively formed only on the electrode where Co is in contact with $CoSi_2$ which has been formed on the substrate. The thus formed cobalt silicide reacts with Si in the $CoSi_2$ on the substrate and accordingly, Co : Si becomes 1 : x ($x \leqq 1$). After the non-reacting Co film and the non-reacting TiN film are removed by wet etching, a thermal treatment is performed under a nitrogen atmosphere at a temperature of 750 ℃ for 30 seconds so that a cobalt silicide layer 15 is converted into a stoichiometric compound ($CoSi_2$) in which Co : Si is 1 : 2 (Figure i). Finally, the thickness of the $CoSi_2$ film 15 is 340 nm. Herein, the $CoSi_2$ film 15 has a resistivity of 25 $\mu\Omega$cm and a sheet resistance of 7.3 Ω/□, which is satisfactory enough since the diffusion layer is required to have a sheet resistance of 10 Ω/□ or less in the logic LSI.

[0016] The thus formed $CoSi_2$ film is significantly different in characteristics from those formed by forming the Co film in total and

subjecting it to a thermal treatment at one time, instead of dividing the $CoSi_2$ formation step. Accordingly, it becomes possible to suppress the increase in a junction leakage current at $CoSi_2$ formation on the respective surfaces of the source and the drain, which has been a problem